

EE 330
Homework 2
Spring 2024
Due Friday Jan 26 at noon

On this and subsequent HW assignments there will be problems that require a Verilog or VHDL solution. It will be assumed that students either have a background in Verilog or VHDL or that they will study what is needed to develop this background. There are numerous sources of material on Hardware Description Languages available online. The text for the course also has a short discussion on HDL in Sec. 1.8 and a more extensive discussion in Appendix A.

Problem 1 (10 pts)

What is the purpose of the DRC and LVS steps in the Cadence design flow?

Problem 2 (10 pts)

Assume the cost per good die is \$3 and the die come from a wafer that is a 45cm diameter wafer which costs \$4000 per wafer. The die size is 0.5 cm^2 . What is the yield of the die? (neglect die loss on the edges of the wafer)

Problem 3 (10 pts)

Assume a 300mm wafers cost \$3200. If the defect density on this wafer is $0.8/\text{cm}^2$, determine the cost per good die if the die is square with a side dimension of 6 mm. Assume the soft yield is 100%.

Problem 4 (10 pts)

Determine the soft yield of a device that has a current bias requirement of 1mA to 3mA if the current bias has a Gaussian distribution with a standard deviation of 0.3mA and a mean of 2mA. How does the soft yield change if the mean is 1.5mA?

Problem 5 (10 pts)

Assume a particular function in a 14nm process being used today requires a die area of 0.25cm^2 and that it is fabricated on 300mm wafers. Predictions suggest that in a few years, high-end processes will have 3nm feature sizes on 450mm wafers. Assuming the circuit schematic does not change but the transistor sizes scale with feature size, how large will the die area be on the new 3nm process? How many die will you be able to fit on the 450mm wafer if waste due to wafer edge and saw lanes are neglected?

Problem 6 (10 pts)

Assume you are an engineer working on IC fabrication for a large semiconductor company. You are told that a new circuit for a Delta-Sigma ADC is in the works and that its die is anticipated to have an area of 0.85mm^2 . You also know that wafers processed at your fab house tend to have a defect density of 1cm^{-2} and the chip has a predicted soft yield of 99%.

- What is the hard yield of the die?
- What is the overall yield?
- Assume that the semiconductor company has a policy of not fabricating die that have a yield that is lower than 95%. As specified, is the ADC suitable to be produced in the fab? If so, how much larger could the designers let the die area be before falling below the 95% yield limit? If not, how low of a defect density would a fab need to be able to achieve the 95% yield?

Problem 7 (10 pts)

Assume the specified offset voltage for each of the 2 amplifiers in a “dual” op amp is 5mV (that is, $|V_{os}| < 5\text{mV}$). Determine the soft yield for the “dual” op amp integrated circuit (i.e. both op amps must meet the V_{os} specification) if the standard deviation of the offset voltage for each op amp is 3 mV and the mean is 0V. Assume the offset voltage for each of the 2 amplifiers are uncorrelated and that the distribution of the offset voltages are Gaussian.

Problem 8 (20 pts)

Using ModelSim create a 4-input **NOR** and a 3-input **NAND** gate. Create a test bench for the code to verify the operation of the design. Provide both your code and the test bench results (appropriate results/waveforms). Use the same input signals for verifying the operation of the **AND** and **NOR** gates in the test bench.

- a) Describe what Data Sequence 1 represents
- b) Describe what Data Sequence 2 represents
- c) What does the term “open-drain” mean?
- d) The I²C protocol is noted for not having logic contention. What does this mean?
- e) Why can devices with modestly different logic levels coexist on the same I²C bus?